A24 Cont

a plurality of chips on a surface of a wafer having trenches running through, each said trench formed between said chips; ~~said wafer has trench formed in said wafer and run through said wafer;~~

a filling material filled in said trenches;

metal pads formed on the surface of said wafer;

~~photo sensitive~~ a photosensitive polymer ~~material~~ layer formed on the surface of said wafer and ~~expose~~ exposing said metal pads;

a first conductive layer formed on said metal pads within said ~~photo sensitive~~ photosensitive polymer ~~material~~ layer;

a circuit ~~diagram patterning~~ distribution pattern formed on the top of said ~~photo sensitive~~ photosensitive polymer ~~material~~ layer and said first conductive layer;

a protection layer covered on said circuit ~~diagram~~ distribution pattern, said ~~photo sensitive~~ photosensitive polymer ~~material~~ layer and a portion of said circuit ~~diagram~~ distribution pattern exposed; and

~~a~~—conductive bumps formed on said exposed circuit ~~diagram~~ distribution pattern.

Claim 14 (currently amended): The wafer level package for producing chip size packages according to claim 13, wherein said ~~photo sensitive~~ photosensitive polymer layer comprises ~~EPOXY~~ epoxy.

Claim 15 (currently amended): The wafer level package for producing chip size packages according to claim 13, wherein said ~~photo sensitive~~

A24 cont.

photosensitive polymer layer comprises ~~photo PI~~ photosensitive polyimide.

Claim 16 (currently amended): The wafer level package for producing chip size packages according to claim 13, wherein said filling material comprises ~~EPOXY~~ epoxy.

Claim 17 (currently amended): The wafer level package for producing chip size packages according to claim 13, wherein said protection layer comprises ~~EPOXY~~ epoxy.

Claim 18 (currently amended): The wafer level package for producing chip size packages according to claim 13, wherein said ~~conductive pattern diagram~~ circuit distribution pattern comprises copper.

Claim 19 (currently amended): The wafer level package for producing chip size packages according to claim 13, wherein said conductive bump comprises solders.

Amendments to the Abstract:

The abstract is replaced by a new abstract as follows:

A25

A wafer level package for producing chip size packages is provided. The wafer level package of the present invention includes a